

Patent Application
Docket No. 47079-00092USPT

REMARKS

Reconsideration and allowance are respectfully requested in view of the foregoing amendments and the following remarks.

Claims 1-18 are pending in this application.

Regarding the § 103 Rejection

Claims 1-18 were rejected under 35 U.S.C. § 103(a) for being rendered obvious by Ozeki et al (U.S. Patent No. 5,402,385) in view of Helmbold et al (U.S. Patent No. 5,497,450). Applicant respectfully traverses this rejection.

Applicant respectfully points out that § 706.02(j) of the MPEP recites that there are three necessary elements to establish a *prima facie* case of obviousness as adopted by *In Re Vaeck*. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine the reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed limitation and the reasonable expectation of success must both be found in the prior art and not based on Applicant's disclosure. *In Re Vaeck*, 947 F2nd 488, (Fed. Cir. 1991).

Ozeki et al does not teach decoding an address of the storage medium. To the contrary, Ozeki teaches decoding an address, but the decoded address is an address of an upper portion of an address from an external device that is connected to the input of the decoder of the gate circuit 50. The address line 8 is constituted by upper address lines that do not correspond to the real

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memory among the 26 lines of the memory device. (See Ozeki et al, Col. 5, lines 2-13) As such, Ozeki specifically requires that the address lines that are decoded are address lines that are not used to address the memory device. In all the schematic figures of Ozeki, the address lines that can actually address the memory device are not used to disable the load condition of the data register. This is true even in FIGURES 4 and 5 where the mask ROMs 101 through 103 do not have rewritable memories. (See Col. 6, lines 48-53) Ozeki goes on to explain how when one assumes that the program in the not-rewritable memory ICs 101 to 103 is to be changed partly, then a signal for generating a specific decode value is supplied from the external device to the address terminals A22 to A25 and at the same time a right control signal is supplied from the gate circuit 50 to the memory ICs 101 to 104 through the line 4. Here again Ozeki is very careful not to use the address lines A0 through A21 which address the memory 104, but instead use address lines A22 through A25 that are above a possible address of the flash memory 104. (See Ozeki, Col. 6, line 54 through Col. 8, line 3) As such, there is no suggestion or motivation in Ozeki to decode "an address line of the storage memory" to determine if a "selected address matches an address of the data register" in order to disable "the load condition of the data register".

Helmhold at Col. 8, lines 21-36 teaches a memory protection circuit that only protects a predetermined portion of the address range. That is, information cannot be accidentally written over information stored in the protected area. Helmhold does not teach disabling a load condition of the memory data register when an address of the storage medium is selected by an external device. Instead Helmhold makes it impossible to address the protected memory locations. Applicant respectfully submits that neither of the references provide any suggestion or motivation, either in the references themselves or in the knowledge generally available to one of

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ordinary skill of the art, to modify the reference or combine the reference teachings to decode "an address of the storage medium selected by an external device; and if the selected address matches an address of the data register, disabling the load condition of the data register."

Furthermore, there is no reasonable expectation of any success by combining the cited references. In particular, Ozeki et al uses address lines that do not actually address the memory device. And, Helmbold et al teaches only protecting a predetermined portion of the address range of a memory device, but it does not protect the predetermined portion of the memory addresses by disabling a load condition of the memory data register when an address of the storage medium is selected by an external device. Combining the two references does not provide anything similar to "decoding an address of the storage medium selected by an external device; and if the selected address matches an address of the data register, disabling the load condition of the data register".

Finally, the prior art references, when combined, do not teach or suggest all the claim limitations. Applicant submits that this issue has been clearly discussed above because Ozeki et al does not use the address lines that address the storage medium and Helmbold does not disable the load condition of the data register. As such, Applicant respectfully submits that a *prima facie* case of obviousness has not been made with respect to the invention as presently claimed. Applicant respectfully requests that the § 103 rejection be withdrawn and submits that all claims are ready for allowance.

Should the Examiner have any further questions or comments facilitating allowance, the Examiner is invited to contact Applicant's representative indicated below to further prosecution of this application to allowance and issuance.

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In view of the above, it is believed that this application is in condition for allowance, and such a Notice is respectfully requested.

Respectfully submitted,

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